

FIG. 1 is a block diagram of a memory management unit (MMU) 100, according to one embodiment of the present invention. The MMU 100 includes a directory index 102, a table index 104, and an offset 106. The directory index 102 is connected to a page directory 104, which contains a page directory entry 112. The table index 104 is connected to a page table 106, which contains a page table entry 114. The offset 106 is connected to a page frame 108, which contains a memory location 116. The page directory entry 112 is connected to the page table 106, and the page table entry 114 is connected to the page frame 108. The memory location 116 is connected to the page frame 108. The MMU 100 is also connected to a CR3 110, which contains a page directory base register 112.

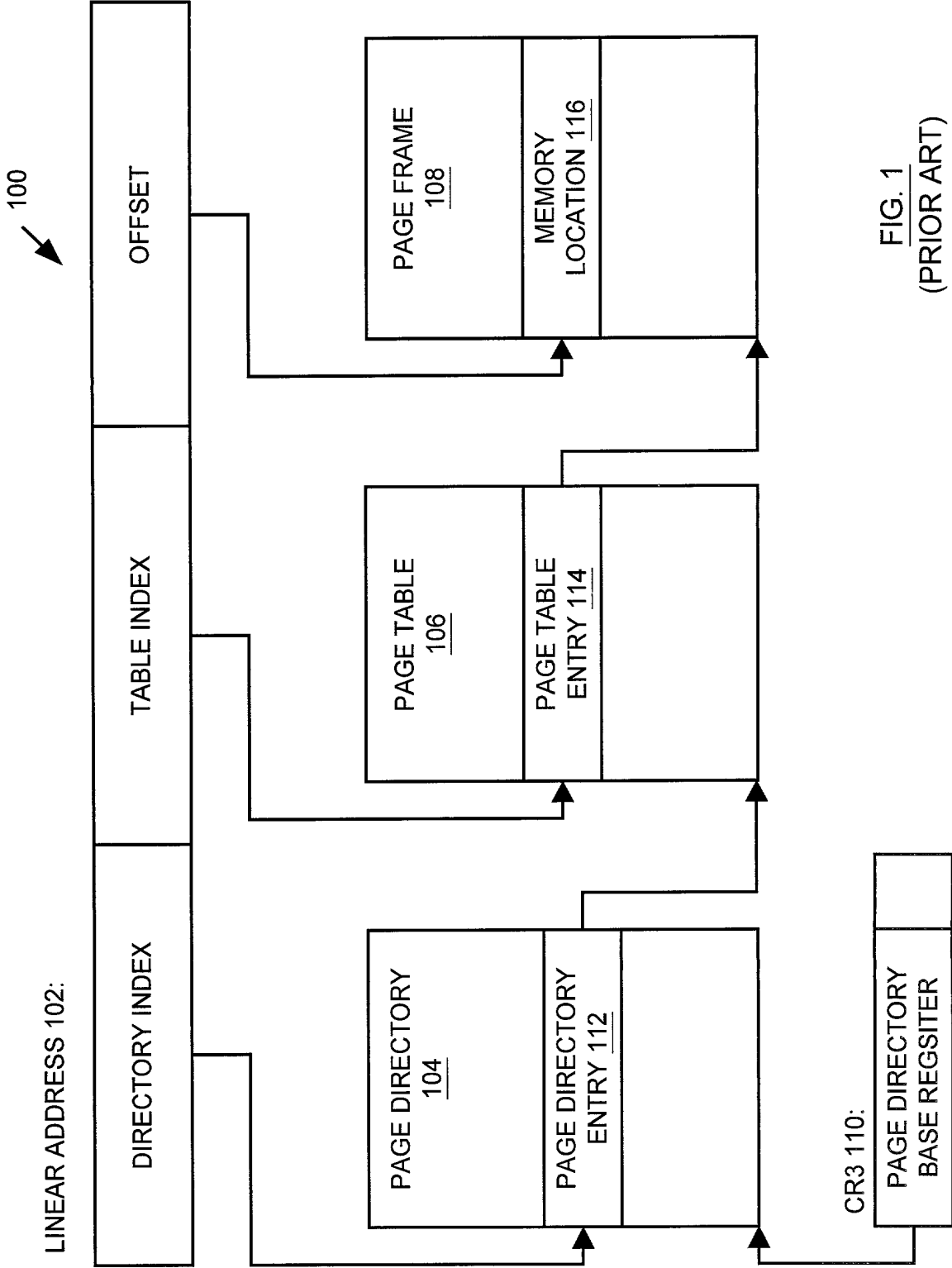


FIG. 1  
(PRIOR ART)

PAGE DIRECTORY ENTRY FORMAT 200:

PAGE TABLE BASE ADDRESS		U / S	R / W	
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FIG. 2  
(PRIOR ART)

PAGE TABLE ENTRY FORMAT 300:

PAGE FRAME BASE ADDRESS		U / S	R / W	
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FIG. 3  
(PRIOR ART)

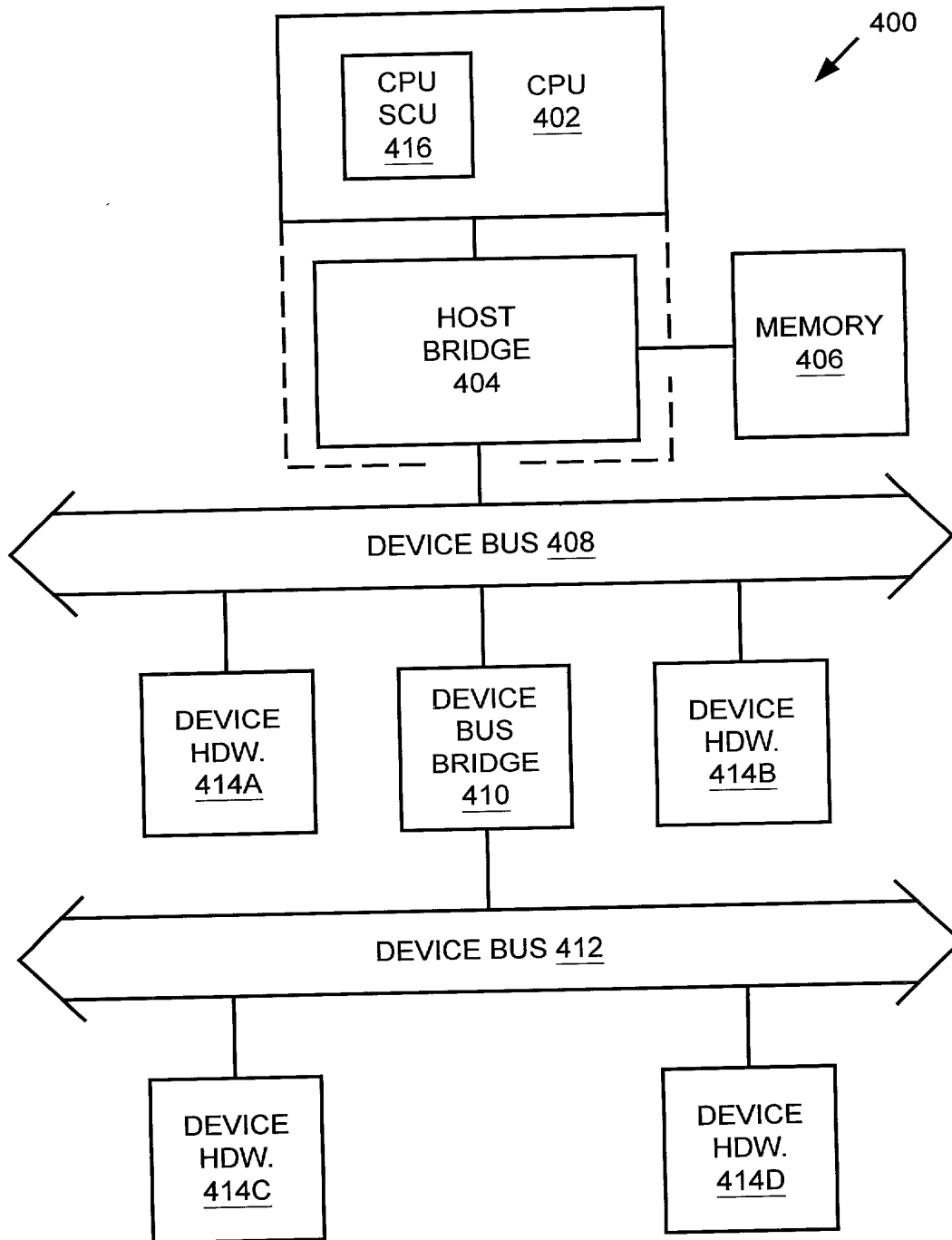


FIG. 4

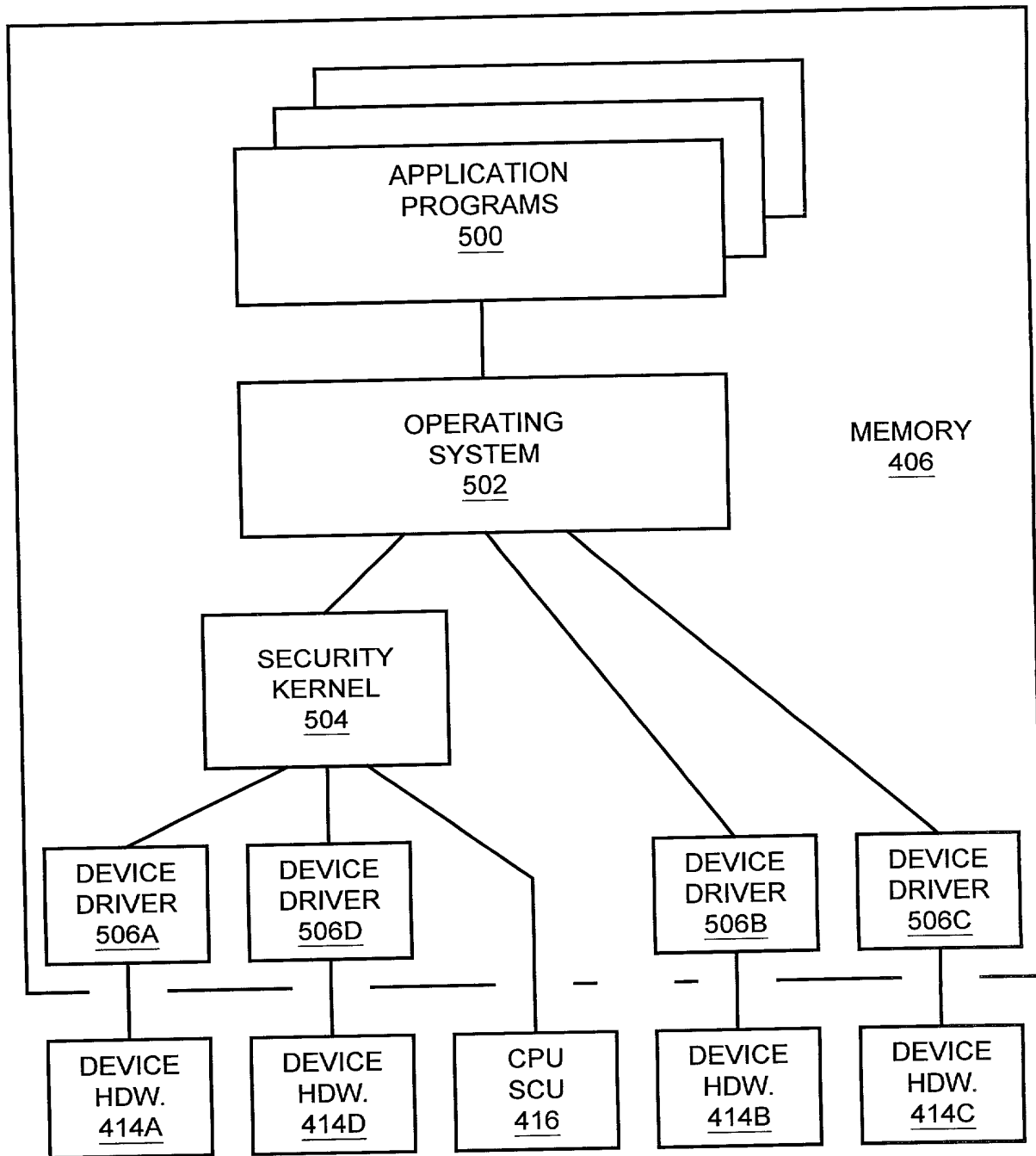


FIG. 5

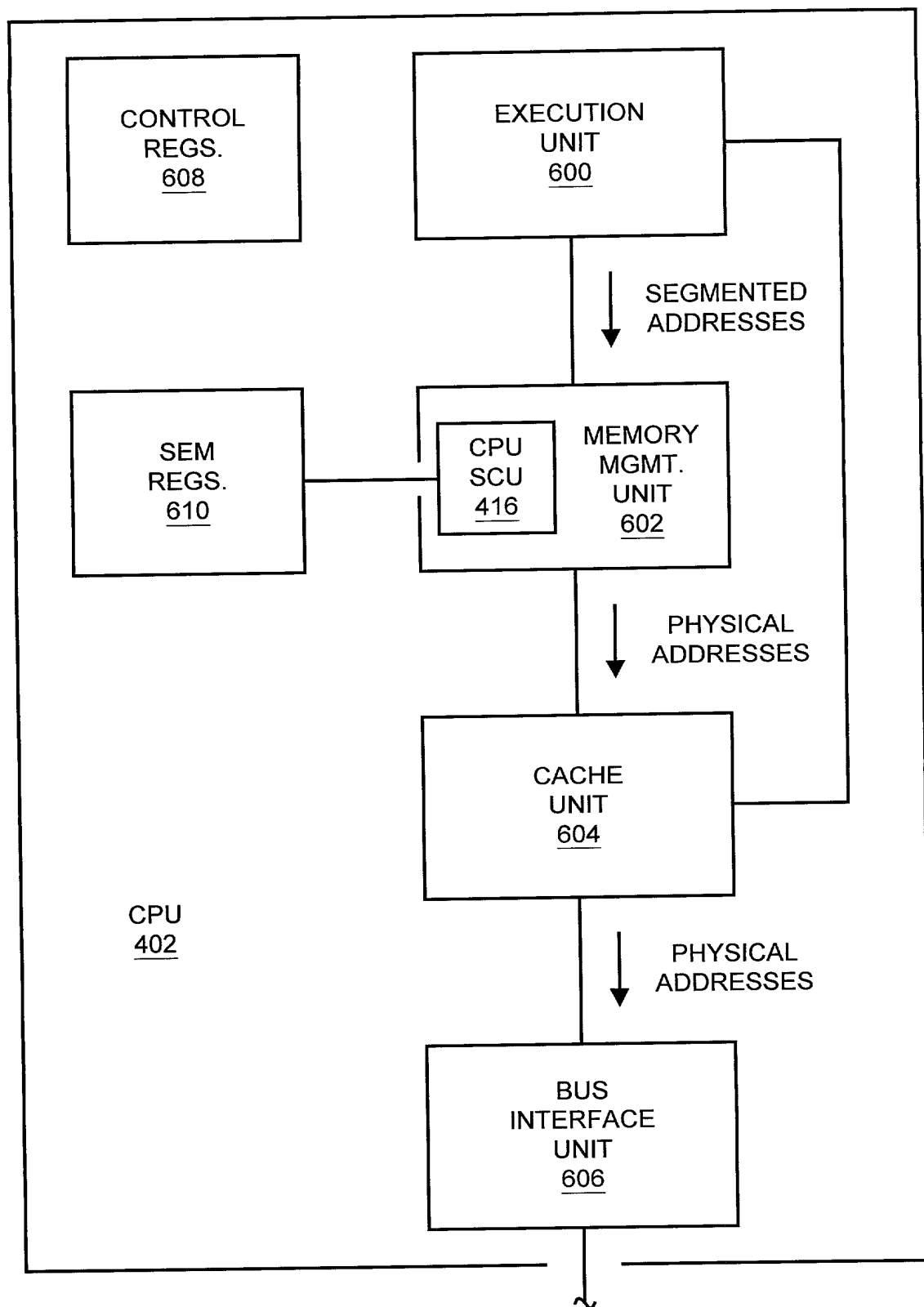


FIG. 6

TO HOST BRIDGE 404

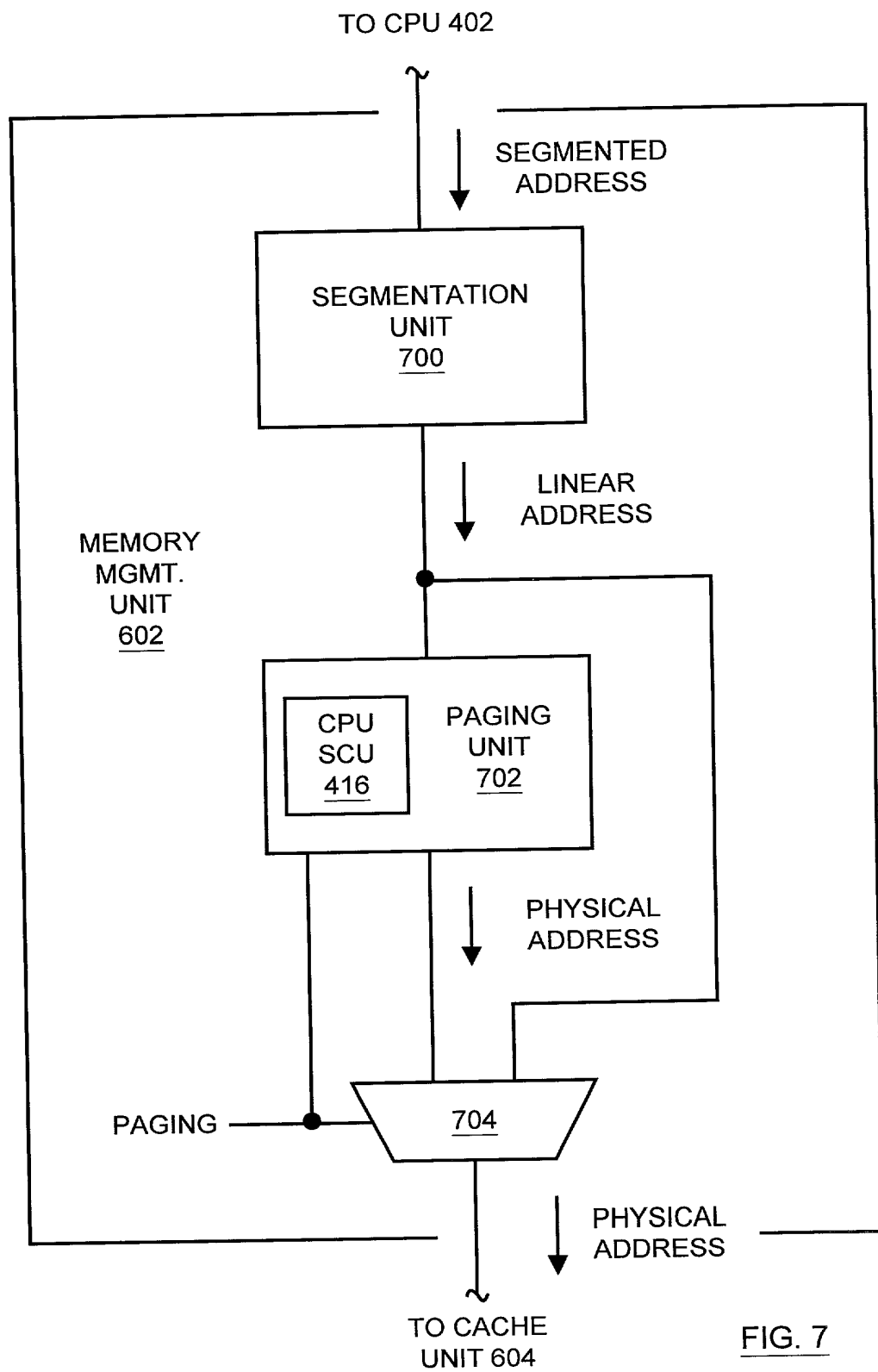


FIG. 7

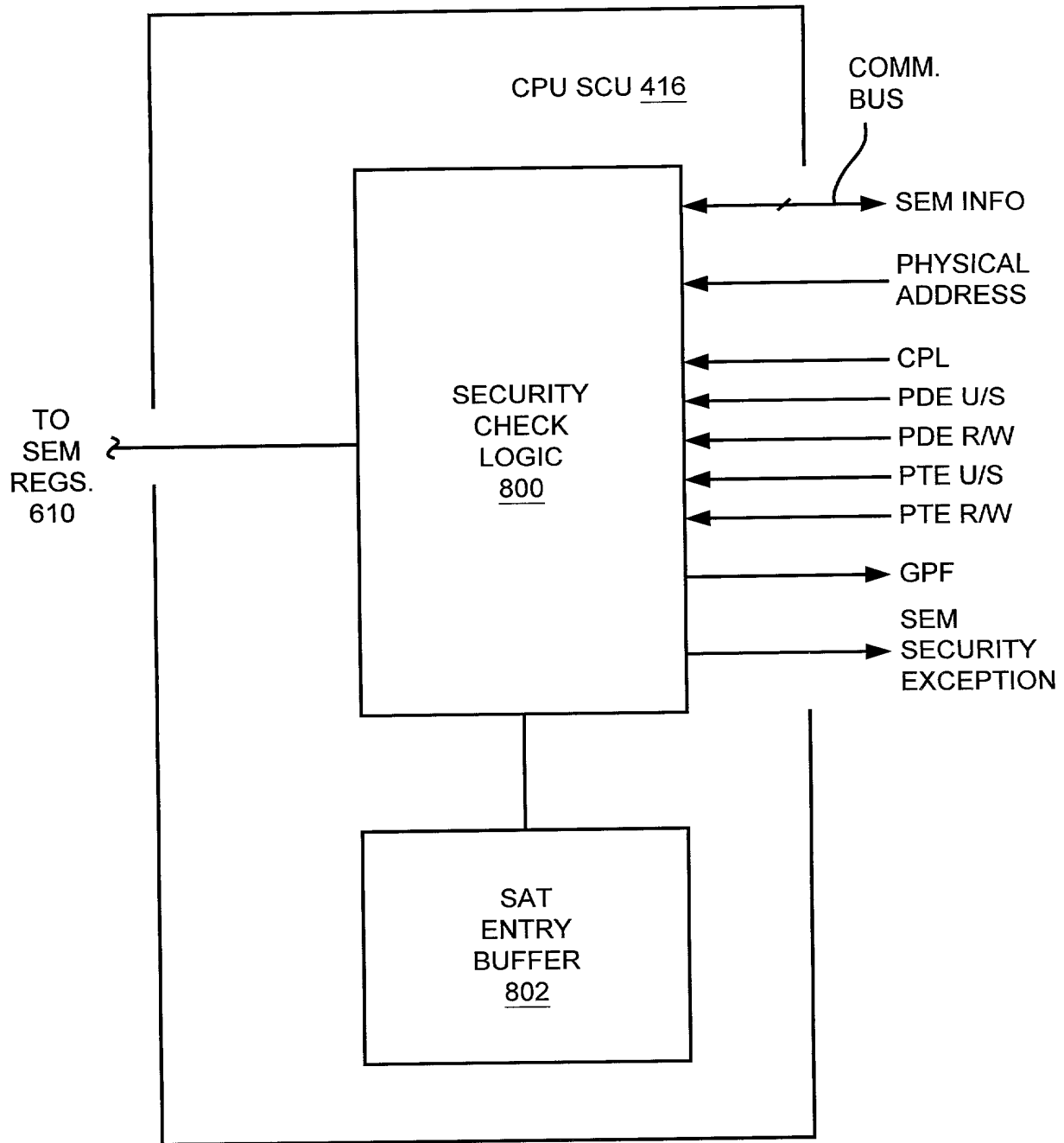
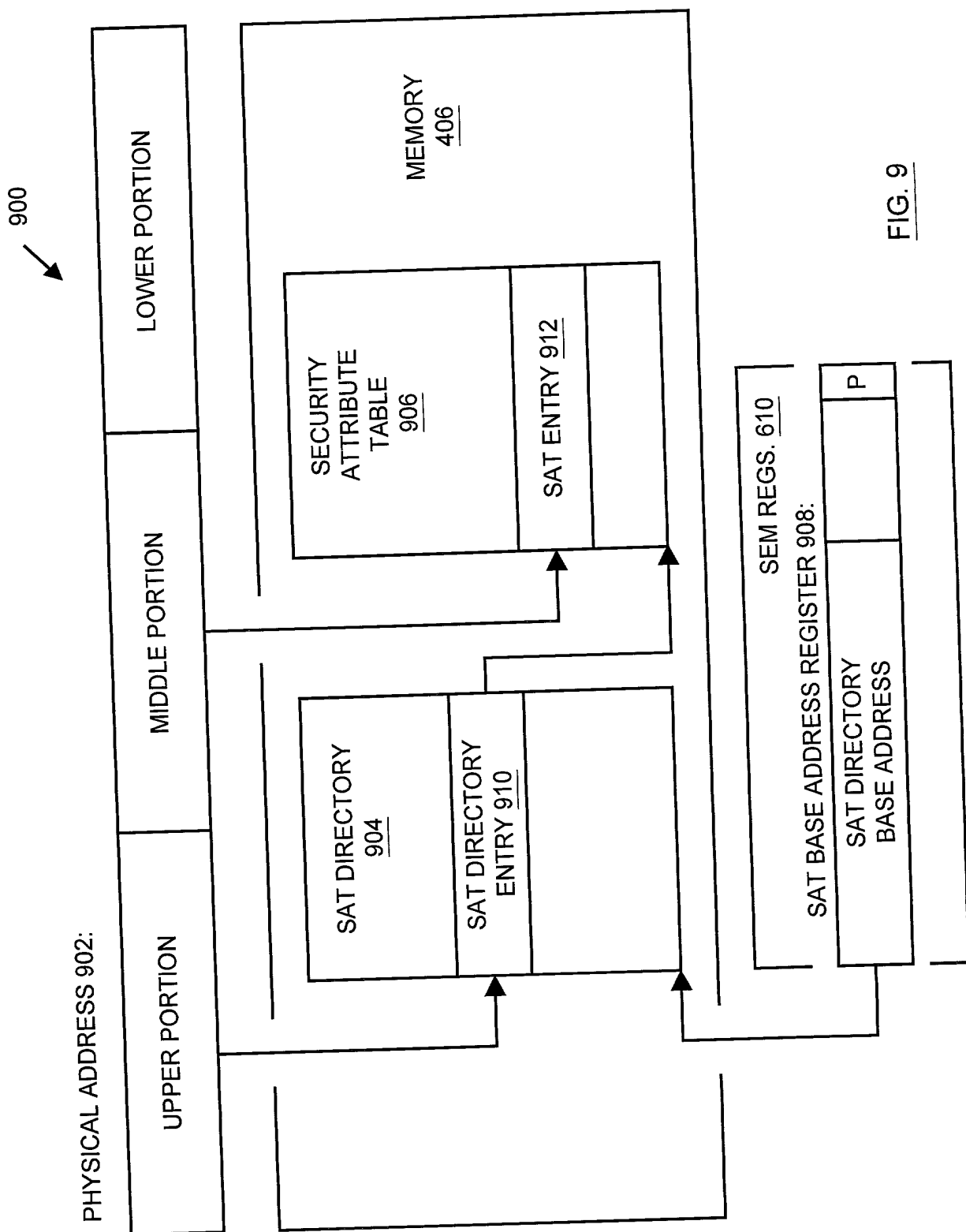


FIG. 8





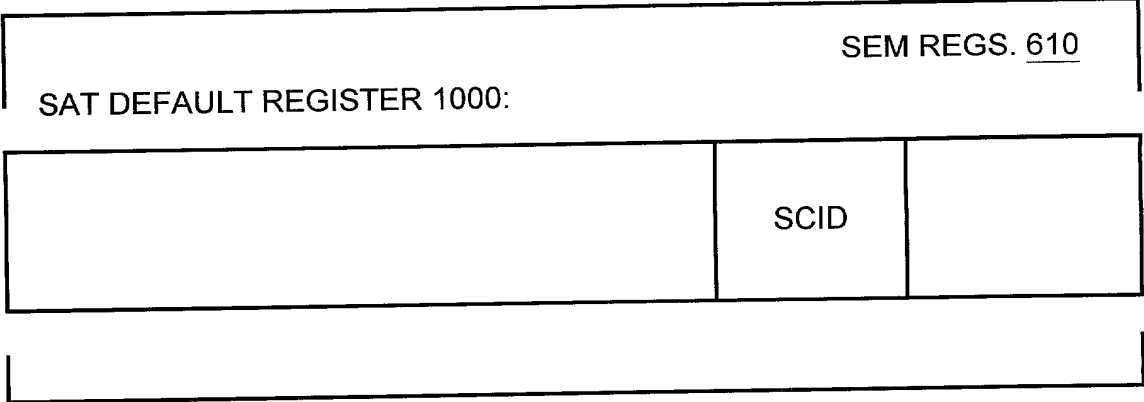


FIG. 10

SAT DIRECTORY ENTRY FORMAT 1100:

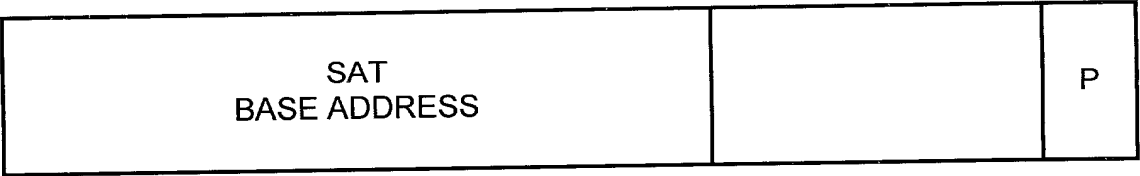


FIG. 11

SAT ENTRY FORMAT 1200:

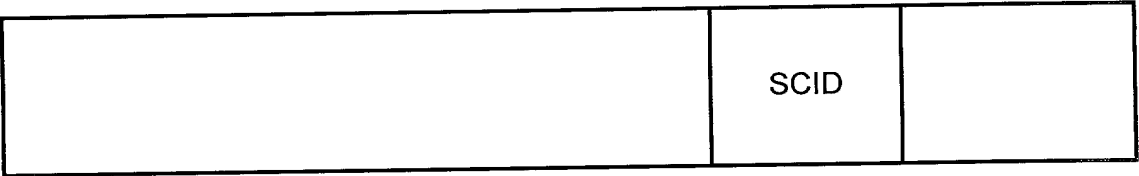
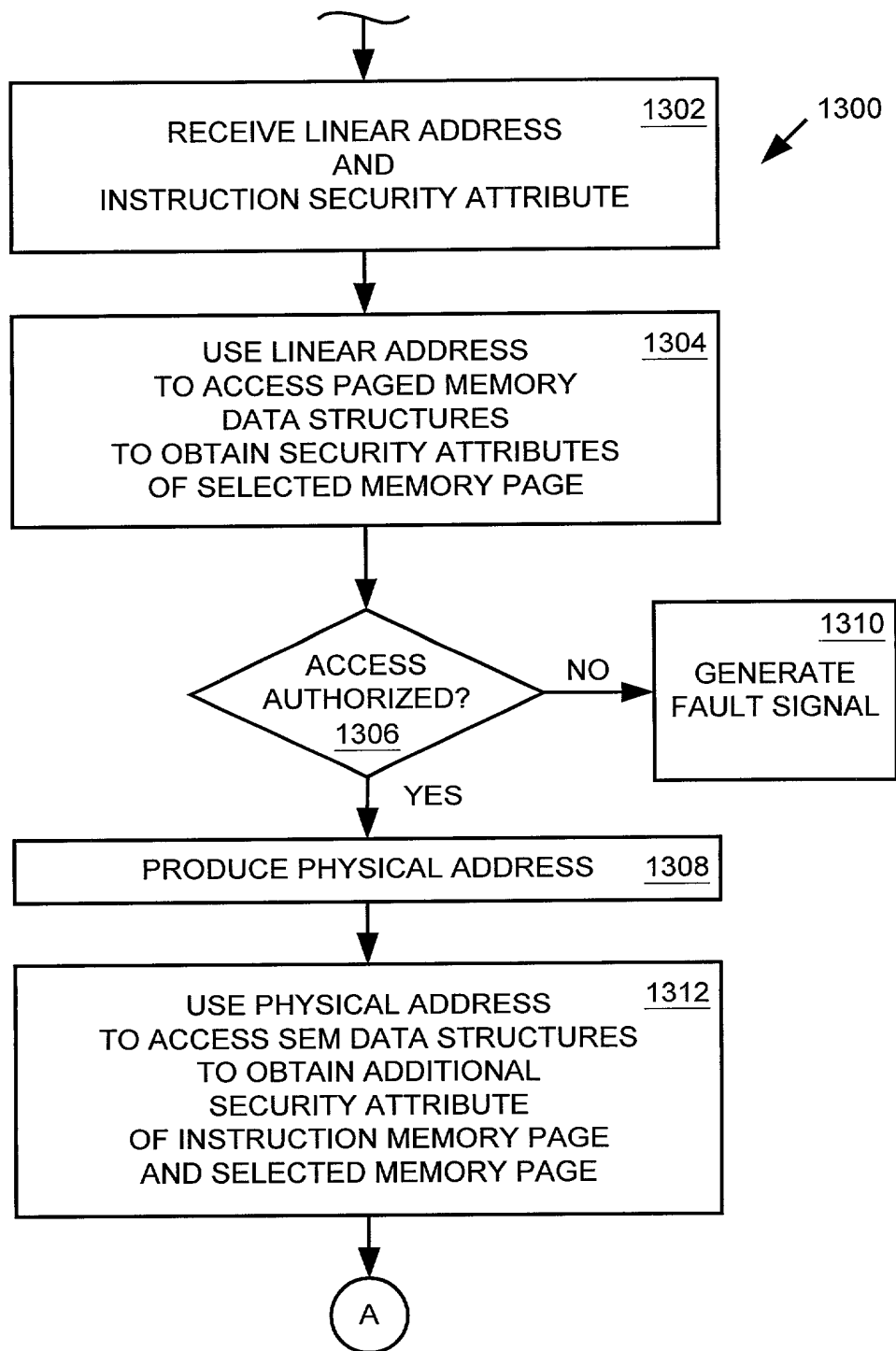


FIG. 12

FIG. 13A



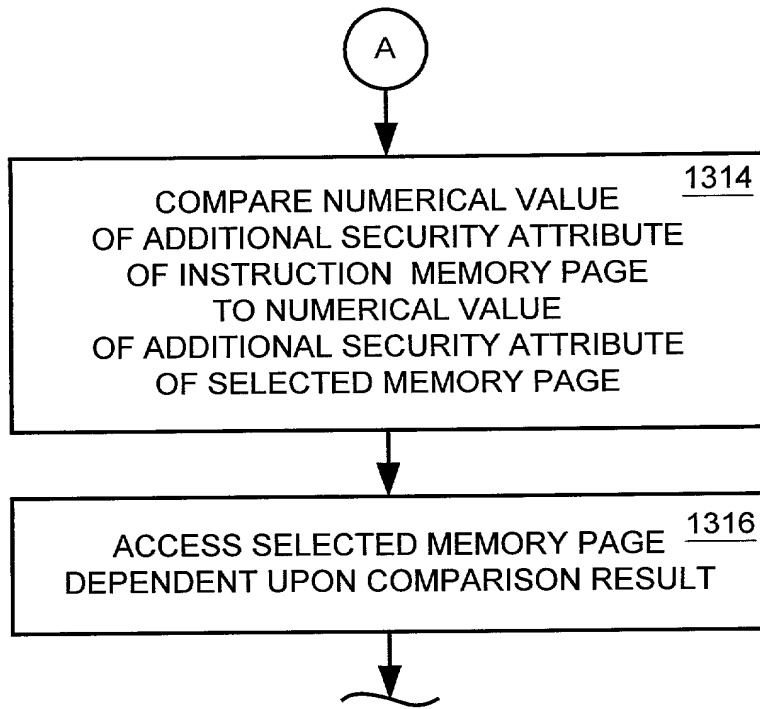


FIG. 13B